CLAIMS

1. A semiconductor package comprising:

at least one plate-like mount;

a semiconductor chip having at least one electrode formed on a top surface thereof, and mounted on said plate-like mount such that a bottom surface of said semiconductor chip is in contact with said plate-like mount;

at least one lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said lead element is spaced apart from the top surface of said semiconductor chip;

a bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said lead element; and

an enveloper sealing and encapsulating said plate-like mount, said semiconductor chip, the inner portion of said lead element, and said bonding-wire element.

2. A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is directly and electrically connected to the second electrode of said semiconductor chip.

3. A semiconductor package as set forth in claim 2, wherein said semiconductor chip is constructed as a MOSFET

chip having a drain electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, with said respective first and second electrodes being defined as a source electrode and a gate electrode, and said plate-like mount has at least one lead element extending therefrom.

4. A semiconductor package as set forth in claim 3, wherein said MOSFET chip is formed as a high power type, and the source electrode has a larger area than that of said gate electrode.

5. A semiconductor package as set forth in claim 4, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

6. A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising: a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is spaced apart from the top surface of said semiconductor chip; and at least one bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said second lead element.

7. A semiconductor package as set forth in claim 6, wherein said semiconductor chip is constructed as a MOSFET chip having a drain electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, with said respective first and second electrodes being

defined as a source electrode and a gate electrode, and said plate-like mount has at least one lead element extending therefrom.

8. A semiconductor package as set forth in claim 7, wherein said MOSFET chip is formed as a high power type, and the source electrode has a larger area than that of said gate electrode.

9. A semiconductor package as set forth in claim 8, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

10. A semiconductor package as set forth in claim 1, wherein said semiconductor chip has another electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, and said plate-like mount has at least one lead element extending therefrom.

11. A semiconductor package as set forth in claim 10, said semiconductor chip is constructed as a diode chip, with one of the electrodes formed on the top and bottom surfaces of said semiconductor chip being defined as an anode electrode, the remaining electrode being defined as a cathode electrode.

12. A semiconductor package as set forth in claim 11, wherein said diode chip is formed as a high power type.

13. A semiconductor package as set forth in claim 12, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

14. A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising: a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is spaced apart from the top surface of said semiconductor chip; and a bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said second lead element.

15. A semiconductor package as set forth in claim 14, said semiconductor chip is constructed as a diode chip, with one of the electrodes formed on the top surface of said semiconductor chip being defined as an anode electrode, the remaining electrode being defined as a cathode electrode.

16. A semiconductor package as set forth in claim 15, wherein said diode chip is formed as a high power type.

17. A semiconductor package as set forth in claim 16, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

18. A production process for manufacturing a semiconductor package, comprising:

preparing a first lead frame having at least one plate-like mount;

mounting a semiconductor chip on said plate-like mount, said semiconductor chip having at least one electrode formed on a top surface thereof;

preparing a second lead frame having at least one lead element, with said lead element having an outer portion, and an inner portion which is previously deformed and shaped with respect to the outer portion;

combining and registering said second lead frame with said first lead frame such that the outer portion of

said lead element is flush with the plate-like mount of said first lead frame, the deformation and shaping of the inner portion of said lead element being performed such that the inner portion thereof overhangs said semiconductor chip, and such that an inner end of said lead element is spaced apart from the top surface of said semiconductor chip;

bonding the electrode of said semiconductor chip and the inner end of said lead element with a bonding-wire element at ends thereof to establish an electrical connection therebetween; and

sealing and encapsulating said plate-like mount, said semiconductor chip, the inner portion of said lead element, and the bonding-wire element in an enveloper.

19. A production process as set forth in claim 18, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said second lead frame having a second lead element having an outer portion, and an inner portion which is previously deformed and shaped with the outer portion of the second lead element, the outer portion of said lead element being flush with the plate-like mount of said first lead frame when combining and registering said second lead frame with said first lead frame, the deformation and shaping of the inner portion of said second lead element being performed such that the inner portion thereof overhangs said semiconductor chip, and such that an inner end of said second lead element is in contact with the second electrode of said semiconductor chip,

said production process further comprising directly and electrically connecting an inner end of said second lead element to the second electrode of said semiconductor chip.

20. A production process as set forth in claim 19, wherein the electrical connection of the inner end of said second lead element to the second electrode of said semiconductor chip is performed by applying an electrically conductive adhesive to the second electrode of said semiconductor chip before the combination and registering of said second lead frame with said first lead frame.

21. A production process as set forth in claim 20, wherein said electrically conductive adhesive is composed of a thermal fusible paste, the electrical connection of the inner end of said second lead element to the second electrode of said semiconductor chip is achieved by further heating the combined first and second lead frames after the combination and registering of said second lead frame with said first lead frame.

22. A production process as set forth in claim 18, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said second lead frame having a second lead element having an outer portion, and an inner portion which is previously deformed and shaped with the outer portion of the second lead element, the outer portion of said lead element being flush with the plate-like mount of said first lead frame when combining and registering said second lead frame with said first lead frame, the deformation and shaping of the inner portion of said second lead element being performed such that the inner portion thereof overhangs said semiconductor chip, and such that an inner end of said second lead element is spaced from the top surface of said semiconductor chip,

said production process further comprising bonding

the second electrode of said semiconductor chip and the inner end of said second lead element with at least one bonding-wire element at ends thereof to establish an electrical connection therebetween.